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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,524	08/07/2001	Chun Wang	ATI.0001670	1770

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 05/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,524	WANG ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. However, in view of the newly discovered references, rejections based on the newly cited references as follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1, 5-19, 21, 24-30, and 32 are rejected under 35 U.S.C. 102(a) as being anticipated by Kilgariff et al. (U.S. Patent No. 5,999,183).

Referring to claims 1 and 6-8, 10, 19, and 21, Kilgariff et al. teach a scalable, three-dimensional (3D) graphics subsystem as shown in Fig. 5, comprising a plurality of graphics modules 500_1 –500_4 coupled together through one or more routing devices. These graphics modules 500_1-500_4 may include the first graphics module 500_1 (shown as module 210 of FIGS. 2-4) and the second graphics module 500_2 (shown as module 410 of FIG. 4) (col. 5, lines 4-24). As shown in FIG. 7, in step 700, a request is transmitted from a requesting agent to read data from memory ("read request") or write data into memory ("write request"). Originating from a requesting agent, the request includes a memory address, a request code to indicate the type of request such as a read, write or acknowledge, and source information which indicates the

graphics module and requesting agent issuing the request (configuration data). In response to receiving the request, the memory controller of the graphics module decodes the memory address to determine whether such address is off-chip (Steps 705 and 710). If the memory address is on-chip, the contents of the address are retrieved (read request) or data is written into dedicated memory associated with that graphics module (Step 715). Otherwise, the memory controller maps the memory address into transfer information including the request code, a device identification (ID) (client ID), local address, source ID, a request number and an optional priority number (Step 720). The "source ID" is the address of the requesting agent and the request number is a number assigned in numeric order to the request in handling out-of-order requests. The "device ID" represents a code indicating which graphics module is targeted to receive the request. The "local address" is the memory address from which data is retrieved or in which data is written (col. 5, lines 53-67, and col. 6, lines 1-23).

In regard to claim 5, as cited above, Kilgariff et al. teach configuration data includes a request number, and further teach the request number is used to ensure that data from multiple responses is processed in order (col. 6, lines 47-48).

As for claim 9, with reference again to Fig. 7, since each rendering module receives access request depending on the local address, client ID, and request number, it is implied that each rendering module process a portion of a request.

Referring to claim 11, as shown in Fig. 4, Kilgariff et al. teach when a rendering module requests access to memory, it decodes the memory address to determine whether the request pertains to content stored in local memory or in remotely located memory. In the later condition, a request is routed through the expansion port targeting the remotely located memory (col. 4,

lines 65-67, and col. 5, lines 1-3). This implies that the request is pending at one memory controller before being transferred to another rendering module.

In regard to claims 12, 14-17, as cited above, Kilgariff et al. teach the configuration data (transfer information) includes a request number and an optional priority number (an identifier). The request number is a number assigned in numeric order to the request in handling out-of-order requests, which implies priority of access request is dynamic.

As for claims 13, 18, and 27, as cited above, Kilgariff et al. teach the transfer information includes an optional priority number and a request number for handling out-of-order requests. Therefore, it is implied that if the requests having equal priority, access requests would be processed in the order to which they are received (round robin arbitration). It is implied that the system should include an internal timer (e.g. a counter) in order to keep track of the number of the request.

Referring to claims 24-26, 29, 30, and 32, as cited above with reference to Fig. 5, Kilgariff et al. teach a scalable graphics subsystem comprising a plurality of rendering modules (clients), each of with includes data access port, a memory controller for receiving input from another rendering module through a router (details of the rendering module shown in Figs. 2 and 3). As shown in Fig. 6, Kilgariff et al. teach a structure of the routing device, wherein each port 630_1-630_4 includes an input and an output. The input is capable of receiving transfer information (defined below) from its corresponding graphics module and of routing that transfer information to any another graphics module or another routing device (col. 5, lines 25-36). As cited above, Kilgariff et al. teach when a rendering module requests access to memory, it decodes the memory address to determine whether the request pertains to content stored in local memory or

in remotely located memory. In the later condition, a request is routed through the expansion port targeting the remotely located memory (col. 4, lines 65-67, and col. 5, lines 1-3), which implies each rendering module having an arbiter. As also cited above, Kilgariff et al. teach the transfer information includes the request code, a device identification (ID) (client ID), local address, source ID, a request number and an optional priority number (programmable values).

In regard to claim 28, Kilgariff et al. teach the transfer information includes an optional priority number and a request number for handling out-of-order requests. Therefore, it is implied that if the requests have equal priorities, access requests would be processed in the order to which they are received (round robin arbitration) (first arbitration), and that if the requests are different in priorities, out-of-order arbitration scheme is implemented (second arbitration).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 35-37, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuboi (U.S. Patent No. 6,414,993).

Referring to claims 35-37, and 39, as shown in Fig. 6, Tsuboi teaches an MPEG decoding system having plural decoders. Three data streams A, B and C are supplied to MPEG video decoders 26/27/28, respectively, and the MPEG video decoders 26/27/28 are respectively associated with frame memories A0/A1/A2, frame memories B0/ B1/B2 and frame memories C0/C1/C2. The frame memories A0-A2, B0-B2 and C0-C2 as a whole constitute a memory 2,

and the memory 2 is connected to a display 3. A synchronous signal generator 4 supplies a synchronous signal to MPEG video controllers 26a/27a/28a forming parts of the MPEG video decoders 26/27/28, respectively. The MPEG video decoder 26 stores the bit strings representative of core pictures and the bit strings representative of B-pictures in the frame memory A0 or A1 and the frame memory A2, respectively, for the data stream A. The MPEG video decoder 27 stores the bit strings representative of core pictures and the bit strings representative of B-pictures in the frame memory B0 or B1 and the frame memory B2, respectively, for the data stream B. The MPEG video decoder 28 stores the bit strings representative of core pictures and the bit strings representative of B-pictures in the frame memory C0 or C1 and the frame memory C2, respectively, for the data stream C. Thus, the MPEG video decoders 26/27/28 process the data streams A, B and C in parallel, and three pictures are reproduced on the display 3 (col. 4, lines 29-38). Therefore, it is implied that the system as taught by Tsuboi having a plurality of memory controllers, each corresponds to an respective MPEG video decoder in order to access respective memories A0-A2, B0-B2, or C0-C2.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kilgariff et al. (U.S. Patent No. 5,999,183).

Referring to claims 2-4, as cited above, Kilgariff et al. teach all the limitations of claims 2-4, including a graphics controller (rendering module), except that the plurality of clients and the plurality of memory controllers are integrated in a single semiconductor device.

However, it would have obvious to one skilled in the art to modify the graphics subsystem as taught by Kilgariff et al. by integrating all the clients and memory controllers in a single semiconductor device, because integrating the components in a single device will increase the speed of the processing device, and also save space.

8. Claims 20, 23, 31, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kilgariff et al. (U.S. Patent No. 5,999,183) in view of Ogata (U.S. Patent No. 4,829,467).

Referring to claims 20, 23, 31, and 34, as cited above, Kilgariff et al. teach all the limitations of claims 20, 23, 31, and 34, except that the number of requests to a memory controller is dependent upon the data of the client, and one of the memory controller can handle high data rate request from client.

However, arbitration of priority which is dependent upon data-rate is well known in the art as described in U.S. Patent No. 4,829,467 to Ogata, which teaches a memory controller 6 (Fig. 1) is constructed to access the data at two different speeds (col. 5, lines 18-22), and further teach the memory controller 6 is constructed to read and write the data from and into the memory at the high speed. As shown in Fig. 4, Ogata teaches a priority order determination circuit of the memory controller. One resource 5' is shared by a plurality of requesters (access means) 1', 2' and 3' and the access competition thereamong is coordinated by priority order determination means 4' in accordance with a priority order in priority order hold means 6'. The priority order

determination means 6' causes priority order change means 7' to change the order in accordance with a degree of the access competition (col. 5, lines 35-53).

Since Kilgariff et al. teach a method of arbitrating among memory controllers with a priority number, Ogata teach a memory controller capable of processing requests of different data rates depending on the priority orders, it would have been obvious to one skilled in the art to utilize the method as taught by Ogata in combination with the method as taught by Kilgariff et al. so that the memory controller can read and write data from and to a memory at a high speed with a simple configuration (col. 3, lines 11-14).

9. Claims 38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuboi (U.S. Patent No. 6,414,993) in view of Ogata (U.S. Patent No. 4,829,467).

Referring to claims 38 and 41, as cited above, Tsuboi teaches all the limitations of claims 18, 20, 23, 31, and 34, except that the number of requests to a memory controller is dependent upon the data of the client, and one of the memory controller can handle high data rate request from client.

However, as cited above, Ogata teaches a memory controller capable of handling high data rate, and of different speeds depending on the priority levels of the requests.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Ogata in combination with the method as taught by Tsuboi so that the memory controller can read and write data from and to a memory at a high speed with a simple configuration (col. 3, lines 11-14).

10. Claims 22 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kilgariff et al. (U.S. Patent No. 5,999,183) in view of Foster et al. (U.S. Patent No. 6,240,492).

Referring to claims 22 and 33, as applied to claims 1 and 24 above, Kilgariff et al. teach all the limitations of claims 22 and 33, except for each memory controller receives an HDTVstream.

However, Foster et al. teach an integrated system architecture 10' for a high definition digital video decoder is depicted in FIG. 2. In this architecture, an integrated circuit chip 12' includes multiple functional units B & C, with generic functional unit A shown to comprise a High Definition Television (HDTV) video decoder 14'. The HDTV video decoder includes two memory ports, with port 1 being coupled to dedicated bus 22 for accessing dedicated memory 26 through dedicated memory controller 24, and port 2 coupled to the general system bus 16 for accessing shared memory 20 through common memory controller 18 (col. 6, lines 19-36).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Foster et al. in combination with the method as taught by Kilgariff et al. in order to minimize costs of the overall architecture and enhance performance (col. 6, lines 40-42).

11. Claim 40 is rejected under 35 U.S.C. 102(e) as being anticipated by Tsuboi (U.S. Patent No. 6,414,993) in view of Foster et al. (U.S. Patent No. 6,240,492).

Referring to claim 40, as applied to claim 35 above, Tsuboi teaches all the limitations of claim 40, except for each MPEG decoder receives an HDTV stream.

However, Foster et al. teach an integrated system architecture 10' for a high definition digital video decoder is depicted in FIG. 2. In this architecture, an integrated circuit chip 12' includes multiple functional units B & C, with generic functional unit A shown to comprise a High Definition Television (HDTV) video decoder 14'. The HDTV video decoder includes two memory ports, with port 1 being coupled to dedicated bus 22 for accessing dedicated memory 26

through dedicated memory controller 24, and port 2 coupled to the general system bus 16 for accessing shared memory 20 through common memory controller 18 (col. 6, lines 19-36).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Foster et al. in combination with the method as taught by Tsuboi in order to minimize costs of the overall architecture and enhance performance (col. 6, lines 40-42).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

05/07/2004

Matthew C. Bella

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